UNITED STATES DISTRICT COURT

EASTERN DISTRICT OF TEXAS

MARSHALL DIVISION

Technology Properties Limited and Patriot Scientific Corporation, Plaintiffs, v. Matsushita Electrical Industrial Co., Ltd., Panasonic Corporation of North America, JVC Americas Corporation, NEC Electronics America, Inc., Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., Toshiba America Information Systems, Inc. and Toshiba America Consumer Products, LLC, Defendants.	§	Case No. 2:05-CV-00494 (TJW) **JURY DEMANDED**

PLAINTIFFS' CLAIM CONSTRUCTION REPLY BRIEF

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I. THE APPLICABLE LAW IS UNDISPUTED

Defendants did not contest or supplement Plaintiffs' statement of claim construction law.

II. THE '336 PATENT[1]

To create non-infringement defenses, Defendants use arguments from the prosecution history, often taken out-of-context, to argue what the claim elements do not cover. However, Defendants' mischaracterizations and omissions show that the inventors did not narrow their claimed invention in the manner Defendants suggest.

In the leading case, *Phillips*, the Federal Circuit downplayed the importance of the prosecution history due to its non-final, shifting, ambiguous nature:

> Yet because the prosecution history represents an ***ongoing negotiation*** between the PTO and the applicant, rather than the final product of that negotiation, it often ***lacks the clarity*** of the specification and thus is ***less useful for claim construction purposes***. See *Inverness Med. Switz. GmbH v. Warner Lambert Co*., 309 F.3d 1373, 1380-82 (Fed.Cir.2002) (the ***ambiguity*** of the prosecution history made it ***less relevant*** to claim construction); *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1580 (Fed.Cir.1996) (the ***ambiguity*** of the prosecution history made it "***unhelpful as an interpretive resource***" for claim construction).

Phillips v. AWH Corp., 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc) (emphasis added).

Defendants' attempted use of the '336 file history shows why the Federal Circuit's concern is justified. This file history included five amendments, at least three telephone conferences (but only one telephone interview summary), at least two principal prior art references − neither of which was confirmed as having been overcome by argument or amendment, and a final examiner interview summary record that only indicates the patent was allowed after the dependent "on-chip input/output interface" limitation was imported into the independent claims, with no link to any prior-art reference. See Exs.[2] 4-12. Thus, Defendants' gratuitous statement that the "entire" clock limitations, "processing frequency" limitations, and

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[1] U.S. Patent No. 5,809,336 (Ex. 1) is referenced herein as the "'336 patent" or just "'336."

[2] All referenced exhibits are attached to one of the Declaration and Supplemental Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief ("Cook"), and will be referenced herein as "Ex. __."

"varying together" limitations "***were required for patentability***" is at best unknowable since there is no statement that the inventors overcame any prior-art rejections by amendment or argument, and because allowability (*i.e.*, patentability) was based on the "I/O interface" limitation. Defendants' 336/'148 Claim Construction Brief, Doc. 226, filed 04/02/2007 ("DBR1") at 9 (emphasis added); Ex. 10; Ex. 11 at 3.

Moreover, Defendants' arguments demonstrate the ambiguity of the '336 file history. For example, in disputing prosecution history arguments about Sheets [*see* Plaintiffs' Claim Construction Brief, Doc. 220, filed 03/19/2007 ("PBR") at 16)], Defendants argue that Plaintiffs mistakenly "assert that this issue has more to do with the variable speed limitation, rather than the ***entire*** clock limitation." DBR1 at 13 n. 8 (emphasis added). ***But the "entire" limitation was not added to the claims until two amendments and over a year after the last discussion of Sheets.*** Exs. 6, 8, 9. A file history so ambiguous cannot support a finding of "clear and unmistakable" intent to surrender invention scope. *See Omega Eng'g, Inc. v. Raytek Corp*., 334 F.3d 1314, 1325-26 (Fed. Cir. 2003).

A. "Entire Ring Oscillator," "Entire Oscillator," and "Entire Variable Speed Clock" Limitations (the "Entire Ring Oscillator" Limitations)

Defendants do not address and therefore concede the flaws Plaintiffs identified in Defendants' use of multiple negative limitations for these terms. *See* PBR at 13. The following discussion is directed to the arguments Defendants ***did*** make.

1. External Crystal

Defendants argue "Plaintiffs assert [ ] that the inventors actually intended to ***cover*** some external crystals in their invention." DBR1 at 7 (emphasis added). This is false. While the "entire ring oscillator" limitations do not ***"cover"*** an external crystal, because they require that the oscillator be on the same semiconductor substrate as the CPU, so long as there is a distinct and separate "entire ring oscillator" on-chip, as the claims actually require, nothing in the file history – including the inventors' statements regarding Magar – prevents that device from ***also having*** an external crystal.

It is undisputed that an external crystal can be used in other ways than taught in Magar,

such as in a delay-locked loop (DLL). Declaration of Alvin M. Despain, Doc. 218, filed 03/19/2007 ("Despain 1") ¶ 51. A DLL does not use an external crystal to directly generate the system clock signal like the crystal oscillator of Magar, but rather to function as a reference signal against which the internal distribution of that reference signal can be compared and "delay-locked," to account for delay across certain circuit elements. *Id.* Given that nothing even remotely related to this functionality was discussed in the '336 prosecution history, the inventors' statements about Magar are not, as the law requires, "a deliberate surrender of claim scope, unmistakable in [their] effect because [they are] not suitable to multiple interpretations." *See Omega*, 334 F.3d at 1327.

Rather than dispute the accuracy of these facts, Defendants dismiss them as mere "technical distinctions," arguing that "none of these distinctions were drawn by the inventors during prosecution." DBR1 at 14. But none of these distinctions were drawn by the inventors during prosecution because the asserted prior art references had nothing to do with this type of use of an external crystal, and therefore Plaintiffs did not "***unequivocally disavow***[]" such uses of an external crystal "***to obtain [their] patent***." *Omega*, 334 F.3d at 1324 (emphasis added). To the extent the statements in the prosecution history are ambiguous, ambiguity must be resolved in the inventors' favor for policy reasons: "To balance the importance of public notice and the right of patentees to seek broad patent coverage, we have thus consistently rejected prosecution statements too vague or ambiguous to qualify as a disavowal of claim scope." *Omega*, 334 F.3d at 1325.

Defendants' own statements belie the alleged irrelevance of Plaintiffs' technical "parsing." Defendants surreptitiously attempt to attribute the technical functionality of a DLL, *i.e.*, the use of an external crystal as a reference signal and the locking of two signals together in some relationship, into Magar and other file-history prior art.[3] Hence, Defendants assert that "the

[3] Defendants' attempt to inject a phase-locked loop (PLL) into the '336 file history through the Edwards patent is particularly egregious. DBR1 at 14 n.9. The Edwards patent, mentioned briefly in the prosecution history, did not actually disclose any oscillator, but the prosecuting attorney assumed it could work with a discrete off-chip crystal oscillator (including the crystal and its "drive circuit") because Edwards teaches a single pin that receives a clock signal.
Continued on the next page

crystal [in Magar] serves as ***a reference signal*** for the clock generator to ***lock*** onto." DBR1 at 7 (emphasis added). Also, Defendants claim that "the inventors distinguished other prior art references . . . including prior art chips in which an off-chip crystal is used ***as a reference signal*** for the on-chip clock circuitry." DBR1 at 12 (emphasis added). But, a "reference signal" and the concept of "locking" have specific technical meanings. Supplemental Declaration of Alvin Despain ("Despain 2"), ¶ 168. For example, locking onto a reference signal typically involves the use of a comparator, which is a circuit element that receives two different inputs (like a reference signal and a second signal), determines the difference between their values, and outputs that difference as a signal. This output signal of the comparator can be used to do different things, like to determine an offsetting delay in conjunction with a DLL, or to phase- or frequency-lock the two signals together using a feedback loop. Despain 2 ¶ 168.

None of this is taught in Magar, which teaches only a traditional crystal oscillator in conjunction with a clock generator circuit to provide internal timing signals. The off-chip crystal in Magar, connected between pins X1 and X2 of an on-chip clock generator only, controls the frequency of the CPU clock.[4] Despain 2 ¶ 165. Tellingly, Defendants' own expert Mr. Gafford does not claim that Magar teaches either a "reference signal" or "locking" functionality, despite being cited in Defendants' brief as support for this proposition. *See* Gafford ¶ 25 (stating only that Magar "controls" the frequency of the clock generator, and is therefore the "dominant

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Despain 2 ¶¶ 167-169. Defendants claim that another patent owned by the same assignee as Edwards ***that was not in the '336 file history and was not identified in the Edwards patent***, and which purportedly teaches a PLL clocking mechanism, was effectively in front of the examiner and the inventors and formed part of the basis of the alleged disclaimer of all uses of an external crystal. (Notably, while Edwards refers to being for use with a "Transputer" microcomputer, this other reference, Talbot, does not use the word "Transputer" once.) Thus, Defendants hypocritically dismiss the technical distinctions made by Plaintiffs, while stretching the facts to simultaneously try to inject those distinctions into the prosecution history.

[4] Contrary to Defendants' assertions (DBR1 at 7), none of the prior-art references discussed in the file history teach uses of an external crystal other than a traditional crystal oscillator. The Edwards patent, discussed in the preceding footnote, does not actually disclose any oscillator. The other two references mentioned by the prosecuting attorney, Palmer and Pohlman et al., teach conventional crystal oscillators. Despain 2 ¶ 169.

influence" on its frequency). Thus, it is undisputed and therefore conceded that the inventors did not clearly and unambiguously disclaim all uses of an external crystal.

2. Control Signal

Defendants never explain their basis for the inventors' alleged disclaimer of any reliance on a "control signal," when the prosecution history only states that the '336 invention does not use a Sheets-type "command input" (*i.e.*, microprocessor command), or other "manual inputs" or "program-controlled inputs," to program the frequency of a voltage-controlled oscillator (VCO). *See* Ex. 6 at 4, Ex. 8 at 5. In fact, Defendants do not even acknowledge the distinction between a "control signal" and "command input," ignoring that a control signal, *e.g.*, the voltage signal to a ***voltage-controlled*** oscillator, would be broader than a Sheets-type microprocessor command input. Despain 1 ¶¶ 53-54; DBR1 at 10, 13-14, 26. Perhaps most revealing, Defendants even claim that "[t]he inventors clearly and unambiguously disclaimed any use of ***external signals*** . . . as part of the CPU clock." [DBR1 at 14 (emphasis added)]; however, since power and ground are external signals, this would exclude a working oscillator altogether!

3. External Clock Generator

Defendants did not disclaim an external clock generator. Defendants do not dispute and therefore concede that an "external clock generator," which is not discussed in the prosecution history, is different than an "external generator" or "external frequency generator," which are mentioned in the prosecution history. *See* PBR at 18-19; Despain 1 ¶ 57. An external frequency generator (or external generator) is simply an off-chip oscillator, such as the external crystal oscillator described in conjunction with the Edwards patent (*see* Ex. 8 at 4), whereas a clock generator is a means to modify the output of an oscillator, such as the "clock gen" circuit of Magar. Despain 1 ¶ 57.

Defendants use these terms correctly when they state that "Magar discloses that the clock generator relies on an external crystal (or ***external generator***) connected to the pins X1 and X2," but incorrectly when they state that "[t]he inventors further distinguished the claims over Sheets by arguing that Sheets used an ***external clock generator***, such as an external voltage controlled oscillator." DBR1 at 13 (emphasis added). With no discussion in the file history of an external

clock generator, there is no basis for a deliberate surrender of this type of circuit from the scope of the claims.

B. "Processing Frequency Capability" and "Processing Frequency"

Defendants continue to insist that features of the preferred embodiment, *i.e.*, the concept of the "fastest safe operating speed," be read into all the claims as a limitation, despite the Federal Circuit's admonishments that this is legal error. *NCube Corp. v. Seachange, Int'l, Inc.*, 426 F.3d 1317, 1321 (Fed. Cir. 2006). There is nothing in the claims about the fastest safe operating speed, with one exception. In claims 1-2, the "processing frequency capability" of the CPU varies together with a speed of the ring oscillator. Plaintiffs propose construing "processing frequency capability" as "the range of speeds at which the CPU can operate,"[5] so the upper end of this range is analogous to the fastest safe operating speed at which the CPU can operate. Thus, claim 1 specifically addresses the ***capability***[6] of a CPU to run at its maximum speed, and addresses changes in the "maximum theoretical performance" (*see* '336, 16:50-54) that vary with changes in temperature, voltage, etc. Thus, the inventors specifically limited their claims to effects on the maximum theoretical performance, but not to the "fastest safe operating speed."

Defendants will not even acknowledge that different claims specify different features of the CPU that vary together with features of the ring oscillator or oscillator, despite the fact that claims 1-2 refer to the "processing frequency capability" of the CPU, claims 3-5 refer to "operating characteristics of electronic devices included within the microprocessor," claims 6-9 refer to "processing frequency of [a] first plurality of electronic devices" of the CPU, and claim 10 refers to the "processing frequency" of the CPU. '336, 32:12-34:27. Thus, Defendants' "one-

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[5] To the extent Defendants cannot understand how a range can vary together with a speed, *see* DBR1 at 19, the answer is simple, based on the Plaintiffs' definition for "vary together": both increase or both decrease. In other words, *e.g.*, the range increases as the maximum theoretical performance increases, varying together with an increase in the speed of the ring oscillator.

[6] The Defendants ignore that claims 1-2 explicitly refer to variations in the processing frequency "capability" of the CPU, instead arguing that Plaintiffs are merely suggesting that a "goal" of the invention is the capability to operate at its fastest safe operating speed. DBR1 at 20 n. 11. However, Plaintiffs never argue that this is a "goal" of the invention, while claims 1-2 do ***explicitly claim*** variations in the processing frequency ***capability*** of the CPU.

size fits all" approach of reading limitations from the preferred embodiment into all claims is not consistent with the inventors' rights to claim their invention broadly, and separately and distinctly by claim. *See Omega*, 334 F.3d at 1325-26; 35 U.S.C. § 112 ¶ 2. Moreover, Defendants' constructions themselves offer no real distinction between "processing frequency" and "processing frequency capability." If the former is the "fastest safe operating speed," and the latter is the "fastest safe operating speed at which the CPU can operate," but the CPU always executes at its fastest safe operating speed, *see* DBR1 at 17-18, then what is the difference between Defendants' definitions for these distinct claim elements?

In arguing that the '336 specification requires that the CPU "always" execute at the maximum frequency possible (*see* DBR1 at 20-21), Defendants misunderstand the '336 patent -- interpreting a statement about the preferred embodiment, that the CPU will "always" (*i.e.*, at any given point in time) execute at the maximum frequency possible, as a mandatory requirement of all embodiments within the scope of the claims. *See* '336, 17:1-2. But, as described above, the inventors clearly decided to claim functionality related to the maximum theoretical performance in some claims, but not others, and thus a description of the preferred embodiment should not be read as a limitation of all of the claims.

Finally, Defendants assert that Plaintiffs' construction of "processing frequency" – the speed at which the CPU operates – is nonsensical because it is identical to the speed at which the ring oscillator / oscillator / variable speed clock operates (*i.e.*, the clock rate). DBR1 at 18-19. But, Defendants mistakenly assume that the speed of the CPU is the same as the clock rate. It is not. While these two parameters may bear some relationship, they are not identical. For example, if one adds RAM memory to his or her computer (*e.g.*, upgrading RAM from 256MB to 2GB), the performance of the computer gets better, programs start up faster, etc., ***yet the clock rate has not changed***. The basis for Defendants' mistaken views on this point appears to be Gafford ¶¶ 8 and 10,[7] stating that "***[u]p to a certain limit***, the faster the microprocessor is

[7] Defendants cite ¶ 18 of Mr. Gafford's declaration for the proposition that a microprocessor always runs at the speed at which it is clocked, but this appears to be in error. Paragraphs 8 and 10 appear to be the supporting paragraphs.

clocked, the greater its computer power will be, and the more useful work it will be able to do. . . . [and] the speed at which a clocked CPU actually operates is therefore the clock speed" (emphasis added). But, in this statement, Mr. Gafford implicitly acknowledges that the speed of the CPU and the clock rate cannot be the same thing because they diverge after a "certain limit."

C. "Varying Together," "Vary Together," Varying . . . in the Same Way," and "Varying in the Same Way" (Collectively, the "Vary Together" Limitations)

Defendants argue that Plaintiffs' construction could not be correct because it would encompass a 50 MHz increase in the CPU processing frequency capability and a corresponding clock rate increase of only 1 MHz, which "could not possibly constitute 'varying together' − the two are not in harmony." DBR1 at 22. Plaintiffs disagree, since changes of this magnitude could constitute "varying together" under the teachings of the '336 patent. Assuming the CPU and the ring oscillator are actually operating at speeds of 1 GHz (*i.e.* 1000 MHz) or higher, a 50 MHz variation would only be 5% of the operating frequency, while a 1 MHz variation would only be 0.1% of the operating frequency. A person of ordinary skill would expect these variations could be +/- 5% for a 1 GHz or faster CPU. Despain 2 ¶ 171. It is not the magnitude of the difference between these changes that is important, but rather that the changes in these parameters occur ***in the same*** direction – *i.e.*, both increase or both decrease. *Id.*; *see also* Despain 1 ¶ 70.

Defendants assert that it is possible for the clock rate of the ring oscillator to exceed the maximum theoretical performance of the CPU, in which case the CPU would become inoperable. DBR1 at 23; Gafford ¶ 21. However, if a person of ordinary skill follows the teachings of the '336 patent, this crossover point will never occur. This is because, if that person chooses to operate the CPU in accordance with its maximum theoretical performance, "CPU 70 will always execute at the maximum frequency possible, but never too fast." '336, 17:1-2; Despain 2 ¶ 172. Because the ring oscillator and the CPU are located on the same integrated circuit substrate, the clock rate and the CPU processing frequency vary together. '336, 17:1-10.

Defendants' arguments illustrate why their 1-to-1 correspondence definition is unrealistic. In the graph of "Defendants' Interpretation" on page 23 of their brief, Defendants illustrate this 1-

to-1 correspondence with two perfectly straight, perfectly aligned lines with identical slope. However, a person of ordinary skill would recognize that this graph does not represent a real-world device, because micro-variations in voltage, temperature, and manufacturing results guarantee these lines would diverge at various points. Despain 1 ¶ 71; Despain 2 ¶ 173.

Defendants implicitly recognize the problems with their construction because they ask the Court to consider an alternative construction (never before raised) that the terms mean "increasing or decreasing commensurately." DBR1 at 24 n. 12. However, "commensurately" is not a technical term, and a person of ordinary skill would not know how to quantify this requirement, nor think to do so. Despain 2 ¶ 174. Instead, that person would avoid these issues and just consider whether the parameters of interest both increase or both decrease, in accordance with Plaintiffs' definition.

D. "Variable Speed" and "Fixed Frequency"

As previously explained, Defendants' definitions are taken directly from a statement made by the prosecuting attorney about ***crystals*** − not about what constitutes "variable speed" or "fixed frequency." PBR at 19-20, 29-30. Yet, Defendants treat this statement as the definition of "fixed frequency" generally, and the inverse (opposite) of this statement as the definition of "variable speed" generally. This is akin to saying, illogically, that all fixed frequency devices are crystals, and all variable speed devices are not crystals.

The prosecuting attorney explained that the fact that a crystal oscillates at a fixed frequency is a property of how the crystal is manufactured, which in turn depends on how it is cut and trimmed, among other factors. Ex. 8 at 4. Thus, these crystal-specific properties are not a proper dividing line between variable-speed and fixed-frequency devices generally. Defining the claim scope around the properties of crystals also ignores other key factors that determine variability of an oscillator, like whether it is on-chip or off-chip, which affects a non-crystal oscillator (made of transistors) differently than a crystal oscillator. *Id*. Thus, a person of ordinary skill would look to distinctions other than whether an oscillator is a crystal or not to determine if its meets these limitations.

Because the '336 patent is clear in what makes an oscillator "variable-speed" as that term

is used in the patent (*i.e.*, capable of operating at speeds that can change), such as being on the same substrate as the CPU, a person of ordinary skill can determine whether an oscillator meets this requirement. While Plaintiffs do not believe fixed frequency needs to be explicitly defined, if the Court deems it necessary, the easiest dividing line[8] between the two concepts is that oscillators that do not demonstrate '336-type variability are fixed frequency.

E. "System Clock" and "Oscillator … Clocking"

Plaintiffs' constructions do not read "entire" out of the claims. The word "entire" is properly applied in construing the various phrases containing "entire …." *See* PBR at 12-19; §II.D above. If the "entire" limitation in a claim is not met, a product would not infringe that claim, since the terms "system clock" or "oscillator … clocking" appear in the claims only in reference to elements to which the "entire" limitation applies. Defendants are simply grasping at an opportunity to shoehorn in another unwarranted exclusion.

To support their position that these phrases must somehow incorporate "entire," Defendants allude to applicants' remarks distinguishing Magar. DBR 1 at 27. But these remarks state that "while most of Magar's clock (generator) circuitry is on the IC, the ***entire oscillator***, which because [sic] it requires an external crystal is not" and "[a]s a self-contained on-chip circuit, Magar's clock gen[erator] is ***distinguished from an oscillator*** in at least that it lacks the crystal or external generator that it requires." Ex. 9 at 4 (emphasis added). Thus, applicants distinguished Magar's clock generator from an ***oscillator***, not from a ***system clock***. Defendants have shown no record basis for reading "entire" into "system clock" or "oscillator … clocking."

F. "Microprocessor"

Defendants argue that a microprocessor must include a central processing unit. DBR1 at 27-28. The only support for this overly-narrow construction is a number of technical dictionaries. *Id*. As explained in TPL's opening claim construction brief, however, the language of the '336 claims suggests that a microprocessor need not include a CPU. PBR at 9. The

[8] Even Defendants acknowledge "[t]he reality is that no clock can ever have a 100% fixed frequency due to noise and other issues." DBR1 at 25.

extrinsic evidence cited by Defendants cannot be used to support a proposed construction that contradicts the plain meaning of the '336 claims. *Phillips*, 415 F.3d at 1327.

Defendants also argue that a microprocessor need not have an input/output ("I/O") interface. DBR1 at 28. TPL's construction, however, does not require that the microprocessor have an I/O interface, but only that it be capable of interfacing with I/O circuitry (on some external device such as a hard drive, printer or keyboard) or, alternatively, with memory circuitry. Every external device with which the microprocessor communicates must have this I/O circuitry. Despain 1 ¶ 43. Defendants have misunderstood TPL's proposed construction.

Defendants also argue that a microprocessor need not have the ability to connect to an external memory because some microprocessors rely solely on on-chip memory. DBR1 at 28. However, TPL's proposed construction requires that the microprocessor have the capability of interfacing with memory circuitry ***or alternatively with I/O circuitry***. Even in Defendants' example of a microprocessor that relies solely on on-chip memory, the microprocessor would have to communicate with some external device (*i.e.*, the I/O circuitry of that device) in order to perform some useful function. Despain 1 ¶ 43. Again, Defendants have misunderstood TPL's proposed construction of this phrase.

G. "Central Processing Unit"

Defendants concede that a CPU need not be in a computer; however, rather than remove "a computer" from their proposed construction, they add "or microcomputer" after "computer." This is no solution, since a microcomputer is merely a subcategory of computers. Defendants' construction still requires that the CPU be in a computer. For reasons previously given (PBR at 7), all reference to "computer," or " microcomputer" should be excluded.

Since Defendants did not address and therefore concede to TPL's previous argument as to why a CPU should not be required to be ***the central*** electronic circuit in a computer (PBR at 7-8), this limitation should be rejected.

H. "Ring Oscillator"

Defendants concede by not contesting that a ring oscillator has an odd number of "inversions" arranged in a loop. But, Defendants dispute that a ring oscillator requires a

"multiple" odd number of inversions, relying on a figure from Mead & Conway as an indication that a ring oscillator can have a single inverter, ignoring the evidence that this figure is just a model of a ring inverter, including a "δ" element – a ***symbol*** representing delay generally – which is implemented as additional inverters. *See* Ex. U (Lender Decl.) at 234, Fig. 7.8(c); *see also id*. ("The easiest way to build these timers is as chains of inverters.") This textbook excerpt also defines a ring oscillator as "rings of an odd number of ***inversions***" (*i.e.*, plural). DBR1 at 30 (emphasis added). Thus, Mead & Conway does not disclose a one-inverter ring oscillator.

Defendants argue that Plaintiffs' multiple examples in the literature (and the '336 patent) of ring oscillators with three or more inversions are only examples of ring oscillators, "far from *defin[ing]* the term." DBR1 at 30. But, notably, Defendants ignore Plaintiffs' textbook on semiconductor design, *Design of Analog CMOS Integrated Circuits*, which states that a single-stage (*i.e.*, single inverter) ring oscillator does not oscillate because the maximum phase shift around the loop that can be achieved is 270 degrees, whereas 360 degrees is required; "[t]he loop therefore fails to sustain oscillator growth." Ex. 21 at 484, 485. Thus, Razavi unambiguously shows that a ring oscillator ***requires*** a multiple, odd number of inversions.

I. "Second clock," "External clock", and "Independent of"

Defendants misstate Plaintiffs' constructions. Plaintiffs construe "second clock" as "a clock not derived from the first clock" and "external clock" as "a clock not derived from the first clock and which is not originated on the same semiconductor substrate upon which the entire oscillator [or variable speed system clock] is located." The "independent of" limitations in each claim mean "a change in the frequency of the second [or external] clock does not affect the frequency of the first clock."[9]

Defendants accuse Plaintiffs of unduly limiting the claim (DBR1 at 31), when it is Defendants who would do exactly that. For instance, "not originated on the same semiconductor substrate …" merely gives the proper meaning to "external" while avoiding any implication that

[9] "First clock" refers to the output of the ring oscillator system clock, oscillator, or system clock depending on the claim in question. PBR at 28.

the external clock signal is never present on the semiconductor substrate; it is limiting but not ***unduly*** limiting. PBR at 27. That the second (or external) clock is "not derived from the first clock" is a necessary condition to independence, as is fully supported by the record. *Id*. at 26.

Most significantly, Defendants falsely characterize one-way independence as "the narrow meaning." DBR1 at 31. In fact, "two-way independence" is narrower. Logically, the one-way statement "A is independent of B" can be true ***regardless*** of whether "B is independent of A" is also true. Two-way independence requires not only "A is independent of B" but also "B is independent of A." Since the claims state that "[the I/O Clock] is independent of [the CPU Clock]" but ***not*** the reverse, a proper construction should not impose the additional unsupported limitation that the CPU Clock also be independent of the I/O Clock.

III. THE '148 PATENT[10]

A. "Memory" (or "A Memory")

The Defendants provide three arguments in support of their proposed construction of "memory," which excludes registers, cache and column latches.

Defendants first argue that memory must exclude column latches because claim 1 separately recites both "memory" and "column latches." DBR1 at 33. Defendants admit, however, that not all column latches should be excluded from memory ("Defendants fully agree that registers, cache and column latches are considered part of memory when they are included in the storage array"). *Id.* at 34. Furthermore, as explained more fully below, the '148 specification teaches that the column latches are part of the DRAM (which forms the memory in claim 2). '148, 8:65-94. Therefore, Defendants' proposed construction is inconsistent with the patent specification and must be rejected. *Sandisk Corp. v. Memorex Products, Inc.*, 415 F.3d 1278, 1285 (Fed. Cir. 2005) ("A claim construction that excludes a preferred embodiment … 'is rarely, if ever, correct.'…," (*quoting Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996)). Additionally, Defendants' argument regarding the use of the terms "memory" and "column latches" in claim 1 has no bearing whatsoever on whether or not ***registers*** and ***cache*** are

[10] U.S. Patent No. 6,598,148 (Ex. 2) is referenced herein as the "'148 patent" or just "'148."

part of "memory."

Defendants then argue that the '148 specification does not support a construction of "memory" that includes "every isolated and miniscule instance of latch or register on the substrate, many of which could be wholly unrelated to a storage array." DBR1 at 33. This argument evidences a fundamental misunderstanding of the '148 disclosure and the various types of memory described therein. For example, the '148 teaches that the column latches are part of the existing on-chip DRAM circuitry, not part of the CPU. '148, 8:65-9:4 (emphasis added). Thus, column latches are inherently a part of a storage array.[11] *Id*. That column latches are used advantageously by the CPU does not mean that the column latches are part of the CPU.

Finally, as mentioned above, Defendants make a distinction between registers, cache and column latches in ***the storage array***, and those in ***the CPU*** -- according to the defendants, the former is "memory" and the latter is not. This distinction is unwarranted. The '148 discloses many types of storage arrays. For example, the patent discloses on-chip DRAM ('148, 6:9-11:16); two 16x32-bit register arrays and a pair of 1024-bit column latches that provide the equivalent of two 32x32-bit arrays (*Id*. at 9:23-28); and a stack memory hierarchy that includes a latch stack and an on-chip RAM stack. *Id*. at 16:15-19. These are all examples of storage arrays. It is unclear in Defendants' theory which, if any, of these would be part of ***the storage array*** that makes up "memory."[12]

Defendants' proposed construction excludes cache, but Defendants provide no arguments whatsoever in support of this exclusion. The term "cache" merely describes a function for which memory is being used. For example, the '148 teaches using both registers and column latches as cache. '148, 9:5-22. There is no support whatsoever for excluding storage elements from being "memory" solely because of the function they are performing.[13]

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[11] The column latches are part of the control circuitry of the memory. Despain 1 ¶¶ 99-100.

[12] Even more unclear is how to classify, under the Defendants' theory, those registers, cache or column latches that arguably form storage arrays within the CPU.

[13] Excluded cache from "memory" could conceivably exclude even the on-chip DRAM of the preferred embodiment from "memory" if the DRAM were used as cache.

Defendants concede (as they must) that the registers, cache and column latches that exist within the storage array are part of "memory." Defendants' proposed construction, however, excludes all registers, cache and column latches, regardless of where they are located.

For the foregoing reasons, Defendants' proposed construction should be rejected.

B. "Total Area of Said Single Substrate"

Defendants argue that their construction of the "total area" limitations only refers to the area enclosed by the outermost edges "of the ***face*** of the substrate ***upon which the integrated circuit is formed,***" (DBR1 at 35 (emphasis added)) rather than all six sides of the substrate. *Id*. Yet, the language of Defendants' construction is not as limited. Further, Defendants do not explain why the unused portions of the face of the substrate upon which the integrated circuit is formed should be used to calculate the total area, whereas the unused portions on the sides and bottom of the substrate should not be used for this calculation. A person of ordinary skill would be concerned only with the portions of the substrate where there is active circuitry. Despain 1 ¶ 148. Portions of the substrate without active circuitry are ignored, regardless of which face of the substrate is being considered. *Id*. Defendants' proposed construction should be rejected.

C. "The Ring Oscillator Disposed On Said Integrated Circuit Substrate" and "A Ring Oscillator Having A Variable Output Frequency"

These constructions, which combine the constructions for "ring oscillator," "integrated circuit substrate," and "variable speed" should be adopted for the same reasons given with regard to those phrases.

D. "Interface Ports For Interprocessor Communication"

Defendants agree that the issue is whether data "can" be transferred or "is" transferred. They argue that TPL's construction, which requires only that the interface ports be capable of interprocessor communication, would render this claim limitation superfluous. Defendants are mistaken. The '148 shift registers can be used for video output, or alternatively for interprocessor communication. '148, 9:59-61. The '148 achieves this flexibility by its innovative column latch architecture. *Id.* at 9:29-35, 61-64. Thus, as previously explained, the interface ports in the '148 are configurable and capable of interprocessor communication as well as other

types of input and/or output. PBR at 35-36. The '148 claims reflect this flexibility, but do not require that the interface ports actually be used for interprocessor communication – requiring only that they be capable of being configured for such use.

IV. THE '584 PATENT[14]

Claim 29, as allowed, covers no fewer than six disclosed embodiments. Ex. 17 at 6-8. Defendants' constructions fail to cover all of these embodiments and should therefore be rejected.

A. "Instruction Groups"

The parties disagree as to whether every set of instructions that is provided to the instruction register as a unit is an "instruction group." In Defendants' view, whether a set of instructions is an "instruction group" depends on the contents of the set. This view is inconsistent with the plain language of claim 29, which requires:

> providing instruction groups to said instruction register … wherein ***certain of*** said instruction groups include at least one ***instruction that***, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups.

'584, 34:53-59 (emphasis added). This language makes two points abundantly clear. First, the "groupedness" characteristic[15] that Defendants make much of is ascribed to an ***instruction***, not to instruction groups. Second, only ***certain of*** the instruction groups must include an instruction having this characteristic. Defendants' construction ignores the plain language of the claim.

Defendants argue that their construction "gives meaning to three concepts found extensively in the intrinsic record." Defendants' '584 Claim Construction Brief [Doc. 225, filed 04/02/2007 ("DBR2")] at 4. In fact, the intrinsic record provides no basis for importing any of these three concepts into the simple term "instruction groups."

1. "Groupedness" is not characteristic of an "instruction group"[16]

Applicants never stated that instruction groups must possess "groupedness." In their only

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[14] U.S. Patent No. 5,784,584 (Ex. 3) is referenced herein as the "'584 patent" or just "'584."

[15] *I.e.*, locating accessed operands or instructions relative to instruction group boundaries.

[16] Plaintiffs' construction of "predetermined position" incorporates this characteristic. *See* §IV.D.

use of the coined word "groupedness," applicants stated that "***[T]his characteristic is represented in the disclosure by example in various instructions*** that are the subject of the dependent claims. Ex. 17 at 6 (emphasis added). Thus, "groupedness" is not a characteristic of instruction groups but of ***instructions***. Further, the phrase "instruction groups" was in claim 29[17] from its first presentation to the PTO. Ex. 13 at 8. The word "groupedness" was coined in the final amendment and connected to the "predetermined position from a boundary" language. Ex. 17 at 5-6.

Defendants' statement that the PTO rejected Plaintiffs' construction (DBR2 at 8) is misleading. The PTO rejected the language "said operands and instructions being located relative to said instruction groups." Ex. 14 at 7 (underlining in original). Applicants responded by replacing this with "said operand or instruction being located at a predetermined position from a boundary of said instruction groups," *see* Ex. 17 at 5, not by narrowing the meaning of "instruction group" as defined in the specification.

Plaintiffs agree that the "boundary must have some significance to the processing of (***at least some*** of the) instruction groups." DBR2 at 8-9 (emphasis added). But it is the "predetermined position" language in claim 29 that defines the significance that the boundary must have, and even Defendants admit that this language applies only to "certain of said instruction groups," not to all of them.

2. Right-Justified Operands Are Not Required

In defense of their arbitrary requirement of right-justified operands Defendants repeat "'magic,' 'must,' and 'always.'" The "magic" words (DBR2 at 5-6) come from two sentences of the specification. The "magic" applies to one embodiment that "handles operands of 8, 16, or 24 bits using the same op-code," ('584, 16:7-8), which is ***not*** the claimed invention.

In relying on these words, Defendants ignore that "the prosecution history represents an ongoing negotiation." *Phillips*, 415 F.3d at 1317. Here, the negotiation included broadening claim 29 beyond a single embodiment. Claim 29 originally included "selecting, in accordance

[17] Claim 29 was application claim 97. for simplicity, we refer to "claim 29" throughout.

with position in said instruction register of one of said instructions of one of said instruction groups, an operand from said one of said instruction groups." Ex. 13 at 8. This language was ***broadened*** in the next amendment -- removing "in accordance with position in said instruction register …" (Ex. 14 at 7) -- and ultimately ***removed*** from the claim. Ex. 17 at 6. In pointing out that the applicants quoted the "magic" words twice during prosecution, Defendants ignore this context. The first quotation was in reference to three ***dependent*** claims[18] that recited "means for determining a width of said operand." Ex. 14 at 12-13. The second was in relation to only one of the six disclosed embodiments. Ex. 17 at 6-8. Neither can be read as limiting claim 29.

Defendants' other citations to the prosecution history also come from remarks made at a time when claim 29 included the "selecting an operand" language that was later removed. This language thus does not limit claim 29. Moreover, there is no technical basis for requiring "right justified operands," as the same benefits attributed to right-justified operands could be obtained in other ways. Despain 2 ¶¶ 175-185.

3. A "single 32-bit RISC/traditional instruction" can be an "instruction group"

Defendants' construction, "sets of from 1 to a maximum number of instructions …" admits that a single instruction ***can*** be a group.[19] But they propose to exclude a subset of the single-instruction groups, those consisting of "a single 32-bit RISC [or traditional conventional] instruction." DBR2 at 4. This selective exclusion of some but not all 32-bit instructions has no basis in the record.

The one sentence Defendants cite to justify their exclusion ('584, 23:4-7; *see* DBR2 at 13) does not say that a 32-bit instruction cannot be a group.[20] Further, nothing in the record makes ***any distinction*** between different classes of 32-bit instructions. Instead of supporting their

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[18] Application claims 88-90 (*see* Ex. 13), which issued as patent claims 17-19.

[19] This is not a "strained" reading; the specification states that a group can contain just one instruction. '584, 19:17-18.

[20] BRANCH, one of the six disclosed embodiments, can be a 32-bit instruction. *See* '584, 20:41-42; Despain 1 ¶ 117.

arbitrary RISC/non-RISC distinction, Defendants substitute the equally arbitrary word "traditional." DBR2 at 12-13. They extracted this word from Plaintiffs' prior statement that as claimed, "the instruction register holds an 'instruction group' rather than the traditional single instruction." DBR2 at 12, *quoting* PBR at 39. This statement, however, merely contrasts Plaintiffs' proposal that an instruction register holds an "instruction group" with a textbook definition that referred to holding a single instruction. PBR at 38-39. Plaintiffs' statement distinguishes traditional instruction ***registers***, not traditional instructions, from claim 29.

B. "Operands"

Defendants assert that their construction provides "that the operands have the capability to be variable width in some instances." In support, they rely on prosecution-history statements related to non-final versions of claim 29 and to irrelevant dependent claims. As discussed in section §IV.A.2, any requirement of handling variable-width operands was ***removed*** from claim 29 during prosecution. Thus, there is no basis for reading such a limitation into claim 29.

C. "Said instruction groups include at least one instruction that, when executed, causes an access to an operand or instruction or both"

Defendants dispute that "second instruction" is limited to "not the next sequential instruction." The important distinction is between "control flow" instructions, which have the ability to redirect execution to a target instruction that is not the next sequential instruction, and "ordinary" instructions, which lack this ability. Despain 1 ¶¶ 131-133.

Defendants are correct that control flow instructions do not always redirect execution away from the next sequential instruction. DBR2 at 16; *cf.* Despain 1 ¶ 133. But "access to an … instruction" in claim 29 refers exclusively to control flow instructions, as these are the type of instructions applicants identified as causing access to instructions. Ex. 16 at 9.

Plaintiffs would agree to "the instruction being executed causes the CPU to use an immediate operand or redirect execution to an instruction that can be other than the next sequential instruction."

D. "Said operand or instruction being located at a predetermined position from a boundary" and "decoding said at least one instruction to determine said predetermined position"

"[W]hich instruction group has the 'predetermined position'" (DBR2 at 17) misstates the issue. Claim 29 clearly states the ***accessed operand or instruction*** (not a group) is "located at a predetermined position from a boundary of said instruction groups." The real issue is which group's boundary is used to define that predetermined position.

Defendants assert that the word "current" must refer to the accessing group. In support, they cite the '584 Abstract; however, this was written before the claim language was finalized. Ex. 14 at 3.[21] Further, the "ordinary usage" of "current" is not "accessing." "Current" means "occurring or existing at the present time." (Webster's Ninth New Collegiate Dictionary 316 (1998), Ex. 26. Which group is "current" (i.e., currently in the instruction register) depends on when the question is asked because in some of the six disclosed embodiments, the target group replaces the accessing group ***during*** execution.[22] PBR at 42-43; Despain 1 ¶¶ 142-144. Moreover, in at least the case of BRANCH, the "predetermined position" of the target instruction is fixed only relative to the boundary of the ***target*** group, not the accessing group. Despain 1 ¶ 144. Plaintiffs are not contradicting the ordinary usage of "current," but rather clarifying it.

Defendants also object to "without reference to operand or address bits in the accessing instruction" as not being based on the record. In the absence of an express definition for "predetermined," Plaintiffs' construction articulates the concept underlying the six disclosed embodiments of "predetermined position." Put another way, in all six disclosed embodiments, for an instruction with a given opcode,[23] the position of the accessed operand or instruction, relative to the boundary of the group that contains it, is always the same (i.e., predetermined), regardless of any other information the accessing instruction might contain.

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[21] After the abstract was finalized, all of the claims were rejected for indefiniteness. Ex. 15 at 2. The word "current" was never included in the independent claims.

[22] Note that this is not the case for MICROLOOP, where the accessing group and the target group are the same. Thus, "current" is unambiguous in this instance, but not in others.

[23] An "opcode" is the portion of each instruction that specifies the operation to be performed.

Defining "predetermined" in this way does not contradict the definition of "instruction." Stating that "decoding … to determine said predetermined position" is done "without reference to operand or address bits" does not preclude those bits from being used in other aspects of instruction decoding. Despain 1 ¶ 148.

E. "Locating said predetermined position"

Plaintiffs' construction is not circular. The parties agree that "supplying" means "using the results of the locating step ***in the step of transferring the bits*** forming the accessed operand or instruction to the central processing unit." Thus, "using the results of the locating step" corresponds to the claim phrase "using said predetermined location," while "transferring the bits forming the accessed operand or instruction" corresponds to "supplying … said operand or instruction or both." Thus, "locating said predetermined position" refers to establishing the point from which operands or instructions are to be supplied, i.e., transferred to the CPU, at the predetermined position.

Defendants' construction, which is limited to "ascertain[ing] the address of the accessed operand or instruction," would exclude several of the six disclosed embodiments. For instance, neither MICROLOOP nor LOAD-SHORT-LITERAL needs to "ascertain the address" of a target instruction or operand since the target instruction group is already in the instruction register. '584, 14:41-64, 28:61-67. To the extent that ascertaining an address of a target group is necessary for a particular instruction, the ascertaining, as well as providing the target group to the instruction register, would be part of "establishing instruction supply" in the locating step. But ascertaining the address is not always necessary.

Further, even if the "locating" step were to involve ascertaining an address, there is no intrinsic support for excluding run-time addition or subtraction operations on the program counter. The specification clearly states that in one embodiment,

> [t]he microprocessor 50 offers four instructions to redirect execution [and these] instructions take a variable length address operand 8, 16 or 24 bits long. ***The microprocessor 50 next address logic*** treats the three operands similarly by ***adding or subtracting them to the current program counter***.

'584, 11:6-15 (emphasis added). That is, the operand is included with the instruction and is

added or subtracted with the current program counter by logic circuits in the microprocessor. This can only happen ***at run time***. Defendants cite an alternative embodiment, but the intrinsic record provides no basis for choosing either embodiment to the exclusion of the other.

V. AGREED TERMS

Plaintiffs hereby adopt Defendants' constructions of the terms "oscillator" ('336), "integrated circuit substrate" ('148), and "instruction register" ('584) as set forth in the Joint Claim Construction Statement, Doc. No. 204, filed 02/16/2007.

VI. CONCLUSION

For the reasons given, the Court should adopt Plaintiffs' proposed constructions.

DATED: April 9, 2007

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CERTIFICATE OF SERVICE

I hereby certify that counsel of record who are deemed to have consented to electronic service are being served this 9th day of April, 2007, with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3). Any other counsel of record will be served by electronic mail, facsimile transmission and/or first class mail on this same date.

/s/ *Roger L. Cook*
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